IN THE SPECIFICATION

Please replace the paragraph beginning on page 13, line 19, with the following amended paragraph:

As apparent from the figure, the P-LDD region 322 is formed between the dummy gate 318 and the drain region 314. In forming the P-LDD region 322, a layer of photoresist 324 is preferably deposited on the upper surface of the wafer 300, such as by using a conventional photolithographic patterning and etching process. By terminating the photoresist layer 324 at the dummy gate 318, thereby leaving the oxide layer 308 between the dummy gate 318 and the drain region 314 exposed, the P-LDD region 322 formed as a result of the p-implant step will be self-aligned with the dummy gate 318, ~~as~~ and thus will also be self-aligned with the gate 316. This is desirable for accurately controlling the distance between the P-LDD region 322 and the gate, thereby ensuring that a proper electrical conduction path is formed between the buried N-LDD layer 306 and a channel region (not shown) of the LDMOS device.